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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,732	02/13/2002	Leo Mathew	SC11805TP	6370

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FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,732	MATHEW ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,2,4,5,7-12,14-21,24,25 and 34 is/are pending in the application.

4a) Of the above claim(s) 35 and 36 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4,5,7-12,14-21,24,25 and 34 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 13 February 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7-14-03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 35 and 36, newly submitted in the amendment filed June 9, 2004 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: The originally examined species included doping first and second sidewall spacers with two angled implants of opposite conductivity type before the first and second sidewall spacers are physically separated. Claims 35 and 36 are directed to a different species where doping of the first and second sidewall spacers with two angled implants of opposite conductivity type is conducted after the first and second sidewall spacers are physically separated

Since applicant had received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 35 and 36 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 2, 4, 5, 7 – 12, 14, 16 – 25, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al. (USPAT 6472258, Adkisson) in view of Fried et al. (USPUB 2003/0113970, Fried).

With regard to claim 1, Adkisson discloses in figures 1 – 5 a method of forming a vertical double gate semiconductor device. Adkisson discloses in figure 1 providing a semiconductor substrate (10). Adkisson discloses in figure 1 providing a first insulating layer (12) over the semiconductor substrate. Adkisson discloses in figure 1 providing a first semiconductor layer (14) over the first insulating layer. Adkisson discloses in figures 1 and 2, and column 3, lines 3 – 37 removing portions of a first semiconductor layer to form the semiconductor structure having a first sidewall (left side of the middle Si region) and a second sidewall (right side of the middle Si region), wherein the first sidewall is opposite the second sidewall. Adkisson discloses in figure 2 forming a second insulating layer (gate oxide) adjacent the first sidewall and the second sidewall. Adkisson discloses in figure 2 and column 3, lines 41 – 48 providing a second semiconductor layer (20) over and adjacent the semiconductor structure, the second semiconductor layer being elevated in an area overlying the semiconductor structure (not shown: after deposition and before the polishing and recessing steps) and having a non-horizontal surface adjoining the semiconductor structure (vertical surfaces of gate polysilicon sandwiching the gate oxide with the semiconductor structure). Adkisson discloses in figure 2 and column 3, lines 41 – 48 wherein the second semiconductor layer is conductive. Adkisson does not teach implanting the second semiconductor layer in a first area adjacent the semiconductor structure with a first

species and implanting the second semiconductor layer in a second area with a second species. Fried teaches in figure 2b, figure 3b, and paragraph 0031 performing a first directional implant (20) of a first conductivity type (n-type) of a second semiconductor layer (18) from a first predetermined direction. Fried further teaches in figure 3b and paragraph 0031 performing a second directional implant (22) of a second conductivity type (p-type) opposite the first conductivity type of the second semiconductor layer from a second predetermined direction. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the double doping process of Fried in the method of Adkisson in order to make the second semiconductor layer conductive and shift the threshold voltage of the device to be compatible with current state of the art CMOS technology as stated by Fried in paragraph 0007. It is further obvious that the implanting step of Fried must be accomplished before the polishing and recessing steps of Adkisson in order to dope gate electrodes without counterdoping. Adkisson discloses in figure 3, figure 3a, figure 5, figure 5a, column 3, line 61 – column 4, line 24, and column 4, line 65 – column 5, line 12 forming a conductive layer (42 and 50) over the semiconductor structure and the second insulating layer. Adkisson discloses in figure 2 and column 3, lines 40 – 49 removing a portion of the second semiconductor layer to physically separate a first gate region (the region to the right of the first semiconductor) and a second gate region (the region to the left of the first semiconductor). Adkisson discloses in figure 3, figure 3a, figure 5, figure 5a, column 3, line 61 – column 4, line 24, and column 4, line 65 – column 5, line 12 removing a portion of the conductive layer. Adkisson discloses in figure 2 wherein the first gate region is adjacent the first sidewall of the semiconductor structure, and it would have been further obvious in view of Fried that the first gate region would have the first conductivity

type. Adkisson discloses in figure 2 wherein the second gate region is adjacent the second sidewall of the semiconductor structure, and it would have been further obvious in view of Fried that the second gate region would have the second conductivity type. It should be noted that the claim limitation "the semiconductor structure preventing migration of doping species between the first gate region and the second gate region" is an intended use recitation that is met by the combination of Adkisson and Field.

With regard to claim 2, Adkisson discloses in figure 2 and column 3, lines30 – 36 wherein the semiconductor structure is a channel region of the vertical double gate semiconductor device.

With regard to claim 4, Adkisson discloses in figure 2 and column 3, lines 40 – 49 wherein removing the portions of the second semiconductor layer comprises planarizing the conductive layer. Adkisson discloses in figure 5, and column 4, line 65 – column 5, line 12 wherein removing the portions of the conductive layer comprises planarizing the conductive layer.

With regard to claim 5, Adkisson discloses in figure 3a further comprising forming a first current electrode region (right end of first semiconductor layer as seen in the shape resembling an "H") and a second current electrode region (left end of first semiconductor layer)in the semiconductor substrate to implement the vertical double gate semiconductor device as a transistor.

With regard to claim 7, Fried teaches in figure 3b and paragraph 0031 each of the first directional implant and the second directional implant is performed by ion implantation at symmetric opposing angles relative to a top surface of the semiconductor substrate.

With regard to claim 8, Fried teaches in paragraph 0032 further comprising annealing the first gate region and the second gate region after the first directional implant and the second directional implant.

With regard to claim 9, Adkisson teaches in figure 2 and column 3, lines 41 – 49 removing a portion of the conductive layer. It is not clear if Adkisson and Fried teach wherein removing a portion of the conductive layer is performed after performing the first directional implant. It would have been obvious in the method of Adkisson and Fried that the conductive layer would be removed only after performing the first directional implant because the second semiconductor of Adkisson is only referred to as gate material. An intrinsically deposited polysilicon would not be sufficient to act as a gate material of the device in Adkisson, and therefore must be made conductive by implanting and doping through the method of Fried. Therefore, in the method of Adkisson and Fried, the conductive layer would not be formed until after the implantation steps are performed to make the gate material conductive.

With regard to claim 10, Adkisson discloses in figure 3 and column 4, lines 14 – 17 further comprising electrically coupling the first gate region and the second gate region (before etching to form spacers, the gate regions are coupled).

With regard to claim 11, Adkisson discloses in figure 3, figure 3a, figure 5, figure 5a, column 3, line 61 – column 4, line 24, and column 4, line 65 – column 5, line 12 further comprising forming a metal layer as the conductive layer.

With regard to claim 12, Adkisson discloses in figure 5, and column 4, lines 14 – 23 wherein forming the conductive layer comprises forming a silicon layer (layer of polysilicon in column 4, lines 20 – 21) over the first electrode region, the second electrode region, and the

semiconductor structure. Adkisson discloses in figure 5, and column 4, lines 14 – 23 forming a first metal layer (silicide of column 4, line 14) over the silicon layer. Adkisson does not teach heating the semiconductor substrate so that the silicon layer and the first metal layer form a silicide. Salicide processing is a well known technique to form silicide layers. Fried teaches in figures 3b, figure 4b, and paragraph 0032 a salicide technique for forming silicide layers. Fried teaches in figures 3b, figure 4b, and paragraph 0032 wherein forming the forming a first metal layer over a silicon layer (28). Fried teaches in figures 3b, figure 4b, and paragraph 0032 heating the semiconductor substrate (10b) so that the silicon layer and the first metal layer form a silicide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the salicide process of Fried in the method of forming a silicide of Adkisson in order to create a contact that has no abrupt electrical barrier between it and the electrode. Such a contact provides superior electrical connection as is well known in the art.

With regard to claim 13, Adkisson discloses in figure 3, figure 3b, and column 4, lines 16 – 17 removing a portion of the conductive layer to form a first contact for the first electrode region and a second contact for the second electrode region, wherein the first contact and the second contact are electrically isolated from each other.

With regard to claim 14, Adkisson discloses in figures 5 and 5a and column 4, lines 65 – column 5, line 12 wherein removing a portion of the conductive layer comprises planarizing (damascene and conventional contacts) the conductive layer.

With regard to claim 16, Adkisson discloses in figure 3, and column 4, lines 20 – 24 wherein the metal layer further comprises a stack of metal layers (42 and 50).

With regard to claim 17, Adkisson discloses in figures 1 – 5 a method of forming a vertical double gate semiconductor device. Adkisson discloses in figure 1 providing a semiconductor substrate (10). Adkisson discloses in figure 1 forming a first insulating layer (12) over the semiconductor substrate. Adkisson discloses in figure 1 forming a first semiconductor layer (14) on the first insulating layer. Adkisson discloses in figures 1 and 2 etching portions of the first semiconductor layer to form a semiconductor structure (Si) having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall in a first direction. Adkisson discloses in figures 1 – 3a and column 2, lines 48 – 57 forming a source region and a drain region in the semiconductor substrate in a second direction, wherein the first direction is substantially perpendicular the second direction. Adkisson discloses in figure 2 forming a second insulating layer on the first sidewall and the second sidewall. Adkisson discloses in figure 2 and column 3, lines 40 – 49 forming a second semiconductor layer (20) over and adjacent the semiconductor structure and the second insulating layer. Adkisson discloses in figure 2 and column 3, lines 41 – 49 wherein the second semiconductor layer comprises (before polishing and recessing steps disclosed in figure 3, lines 41 – 42) a first semiconductor portion which is adjacent the first sidewall and having a first non-horizontal (vertical) surface, a second semiconductor portion (not shown, before polishing) which is over the semiconductor structure, and a third semiconductor portion which is adjacent the second sidewall and having a second non-horizontal (vertical) surface. Adkisson discloses in figure 2, and column 3, lines 40 – 49 that the gate polysilicon is conductive in order for the device to be capable of working as a semiconductor device. Adkisson does not teach doping by an angular implant the first semiconductor portion and the third semiconductor portion. Fried discloses in figure 3b, and

paragraph 0031 doping (20) a first semiconductor portion (24) with a first species and doping (22) a third semiconductor portion(26) with a second species opposite the first species. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the doping of Fried in the method of Adkisson in order to make the second semiconductor layer conductive and shift the threshold voltage of the device to be compatible with current state of the art CMOS technology as stated by Fried in paragraph 0007. Adkisson discloses in figure 2, and column 3, lines 40 – 49 removing the second semiconductor portion.. It would have been further obvious in the method of Adkisson and Fried the removing the second semiconductor portion would be subsequent to forming the first and second semiconductor portions because the third portion is needed in the formation of the first and second portions and the removal will serve to physically separate the first semiconductor portion and the third semiconductor portion via the semiconductor structure to substantially eliminate migration of doping species between the first semiconductor portion and the third semiconductor portion, the semiconductor structure comprising differing material composition than the first semiconductor portion and the third semiconductor portion at all adjoining surfaces.

With regard to claim 18, Adkisson discloses in column 3, lines 37 - 40 wherein the second insulating layer is deposited conformally (deposited).

With regard to claim 19, Fried teaches in paragraph 0032 further comprising annealing the second semiconductor layer.

With regard to claim 20, Adkisson teaches in figure 2 and column 3, lines 41 – 49 removing the second semiconductor portion. It is not clear if Adkisson and Fried teach wherein removing the second semiconductor portion is performed after doping the second semiconductor

layer. It would have been obvious in the method of Adkisson and Fried that the second semiconductor portion would be removed only after the annealing because the second semiconductor of Adkisson is only referred to as gate material. The deposited polysilicon of Fried would not be sufficient to act as a gate material of the device in Adkisson until the layer is conductive enough to be a gate polysilicon. Therefore, the gate polysilicon must be annealed in the method of Adkisson and Fried before removal of the second semiconductor portion because the annealing is part of forming the gate polysilicon.

With regard to claim 21, Adkisson discloses in column 3, lines 40 – 49 wherein removing the second portion is performed by planarization (polished).

With regard to claim 22, Fried teaches in figure 3b and paragraph 0031 wherein doping the first semiconductor portion and the third semiconductor portion further comprises doping the first semiconductor portion with a first species and doping the third semiconductor portion with a second species, wherein the first species and the second species are different in conductivity.

With regard to claim 23, Fried teaches in figure 3b and paragraph 0031 wherein doping the first semiconductor portion and the third semiconductor portion is performed by ion implanting species at an angle relative to a top surface of the semiconductor substrate.

With regard to claim 24, Fried teaches in figure 3b and paragraph 0031 wherein doping the first semiconductor portion and the third semiconductor portion further includes forming a patterned layer (14) over the semiconductor substrate.

With regard to claim 25, Adkisson discloses in figures 1 and 2; and column 3, lines 20 – 30 wherein etching portions of the first semiconductor layer to form the semiconductor structure further comprises: forming a third insulating layer (thin oxide) over the first semiconductor

layer; forming a nitride layer (SiN) over the third insulating layer; patterning the nitride layer and the third insulating layer; and etching the first semiconductor layer using the nitride layer and the third insulating layer as a mask.

The rejection of claim 34 is similar to the rejection of claims 1 and 17 above using Adkisson in view of Fried.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson and Fried as applied to claims 1 and 11 above, and further in view of Forbes et al. (USPAT 6414356, Forbes).

With regard to claim 15, Adkisson discloses in figures 2 – 3 forming first and second gate regions before forming the metal. Adkisson does not teach further comprising annealing the first gate region and the second gate region before forming the metal. Forbes teaches in figure 4L, figure 4M, figure 5a, column 12, lines 29 – 55, and column 13, lines 16 – 61 annealing a first gate region (463a) and a second electrode region (463b) before forming a metal (560). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the annealing of Forbes in the method of Adkisson and Fried in order to activate dopant species in the gate layer as stated by Forbes in column 12, lines 35 – 55.

Response to Arguments

5. Applicant's arguments filed November 4, 2004 have been fully considered but they are not persuasive.

6. With regard to applicant's argument that "Fried et al. teach a single gate FINFET structure having asymmetric doping. The single gate, for example, is conductive portions 26, 28 and 24 where portion 28 is counter doped and portions 26 and 24 are oppositely doped," it should be noted that the disclosure of Fried is only directed to a double gate device. For example, conductive portion 24 is one gate, oppositely doped portion 26 is the second gate, and counter doped portion 28 is not conductive enough (if at all) to interfere with the first and second gate interaction. Portion 28 is not part of a gate structure that includes the two oppositely doped gates 24 and 26. Fried makes several references to double gated devices in paragraphs [0001], [0004], [0005], and [0007], while only making one reference to a single gated device in the last sentence of paragraph [0005]: "the variation of the threshold voltage with drain voltage and with gate length of a prior art double-gated MOSFET is much smaller than that of a conventional single-gated structure of the same channel length." This sentence is a clear reason why Fried uses a double-gated device instead of a single gated device. Thus, Fried clearly points to the fact that the device is double gated, not single gated. Fried and Adkisson, both being double gated devices, are clearly combinable logically because they are related to the same type of device. Therefore, applicant's arguments are not persuasive and the rejection is proper.

7. With regard to applicant's argument that "the paragraph 0007 teaching of Fried fails to make obvious the rejected claims because of the counter doping issues present in the prior art also are present in the Fried single gate structure," it should be noted that this is an attack against Fried individually. The method of Adkisson and Fried does not result in a counter doped region

in the final device, and Fried is a double gated structure. Adkisson removes the top portion of the polysilicon which, in the combination of Adkisson and Fried, would be the counter doped portion. Thus, the final device of the combination does not have the counter doping issues present in the prior art of applicant's specification. Further, as explained above, Fried is a double-gated device. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Therefore, applicant's arguments are not persuasive and the rejection is proper.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II